UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/541,611	07/07/2005	Satoshi Yamanaka	0925-0220PUS1	8340

2292 7590 05/20/2010
BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
ZHU, RICHARD Z	

ART UNIT	PAPER NUMBER
2625	

NOTIFICATION DATE	DELIVERY MODE
05/20/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/541,611	YAMANAKA ET AL.	
	Examiner	Art Unit	
	RICHARD Z. ZHU	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04/29/2010 has been entered.

Response to Applicant's Arguments

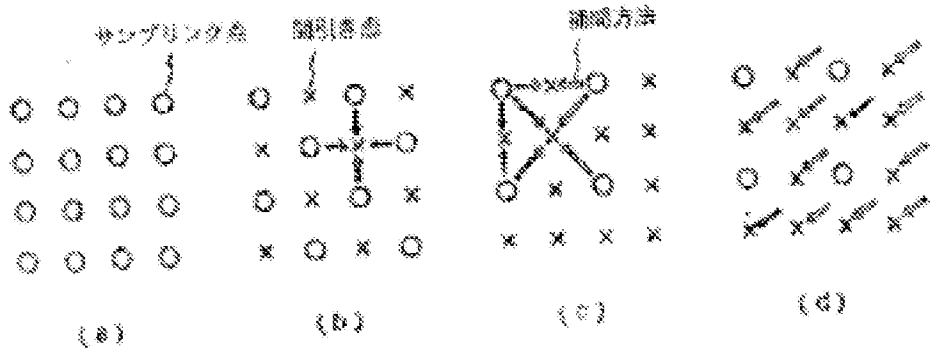
2. **In response to "**Applicants respectfully submit that Ashibe's teachings are directed to block based processing and thus performs a thinning operation determined on a block of pixels and not specific to each "lost" pixel**".**

Ashibe discloses on page 8 of its specification "when an image signal is first input on the transmission side, thining and interpolation for each mode are performed". As best understood by the examiner, ***Ashibe*** is in the art of image compression for optimal transmission over a network with limited bandwidth while taking into consideration the need to preserve image quality. In particular, ***Ashibe*** suggested that for compression purpose, image data are divided into blocks (**Page 6, "an image is divided into blocks having a predetermined size"**) and a number of pixels in each block are thinned (**Page 6, "pixels in**

each block are thinned" and see Fig 3; hence, thinned pixels are assumed to be lost). Although ***Ashibe*** does not go into detail with respect to how pixels are thinned during a compression process and how interpolations of pixels in each block are carried out, however, the examiner believes it is proper to introduce a reference in the very same art of ***Ashibe*** to demonstrate how this process is performed.

Saver (US 5418714 A) discloses a block adaptive image compression (**Col 7, Row 51 – Col 8, Row 6, "divide an image into M x M pixel blocks"**) where "data storage and transmission requirements are reduced by sending a subset of the entire pixel data set existing in an image pixel data set. The pixels that are stored are referred to as primary pixels. The remaining pixels that are not transmitted or stored are referred to as secondary pixels" (**Abstract, it appears that "secondary pixels" are pixels that are thinned or assumed to be lost during the compression process because they are not being transmitted at all**). ***Saver*** further explained that "A high fidelity image can be reproduced utilizing only the primary pixels. The method and apparatus of the present inventions estimates the secondary pixel values from the primary pixel values by predicting that a secondary pixel will look like the surrounding primary pixels, or by interpolating a value for the secondary pixels by summing the surrounding primary pixels and averaging them to obtain a value for the secondary pixel" (**Abstract and see Fig 2**).

It is the position of the examiner that ***Saver*** demonstrated the state of the art ***Ashibe*** is in and it is evidence of inherency for how ***Ashibe*** performs pixel thinning and interpolation for the following reason:



The Japanese character on the top of ***Ashibe***'s Fig 3(c) is roughly translated to mean "reconstruction method" where the specification corresponding to Fig 3 describes Fig 3(a)-Fig 3(d) having compression ratios (thinning ratio) of 0, ½, ¾, and ¾ respectively. The figure demonstrates two facts:

1. "o" pixels are what ***Saver*** refers to as "primary pixels" upon which thinned out pixels or "secondary pixels" are reconstruct or interpolate from.

2. "x" pixels are reconstructed from neighboring "o" pixels.

Therefore, while it is indeed true ***Ashibe***'s teachings are directed to block based processing, however, its thinning / compression and interpolation operation are nevertheless perform on the same unknown interpolation pixel in each block (**See for example the "x" pixel at 3rd column, 2nd row of Figs 3b-3d**).

See detailed rejections below.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-7 are rejected under 35 USC 103(a) as being unpatentable over ***Ashibe et al. (JP 363122385 A)*** in view of ***Saver (US 5418714 A)*** and ***Jiang (US 7242819 B2)***.

Regarding the apparatus of Claim 1 and therefore method of Claim 4, ***Ashibe*** discloses a pixel interpolation circuit (**Drawing 2, Unit 20**) for generating interpolation pixel data which interpolates an input image based on pixel data composing the input image (**See Abstract**), the pixel interpolation circuit comprising:

an interpolation unit (**Drawing 2, Unit 20**) for calculating interpolation candidate data of the same unknown interpolation pixel for each unknown interpolation pixel (**For example, pixel "x" at 3rd column, 2nd row of Fig 3(b)-(d). See also Page 8, "when an image signal is first input on the transmission side, thinning and interpolation for each mode are performed"**) based on calculations performed on test interpolation data of a plurality of normal pixels neighboring the interpolation pixel (**Drawing 3, "o" are normal pixels neighboring interpolation pixels "x", see Abstract "initially, interpolation to respective modes are carried out". Particularly 3(c) where "x" is interpolated using neighboring "o"**), where each interpolation candidate data is to be interpolated using different interpolation methods (**Abstract, "the four types of thinning out and interpolating methods shown in the drawings (a)-(d)", see Drawing 3**), wherein said test

interpolation data is calculated for each of said normal pixels on the assumption that said normal pixels are lost using said different interpolation methods (**Abstract, "Then, the sum in the block of the absolute value of the difference between an interpolation signal and an original signal, namely, the quantity of the distortion to the respective modes for every block is calculates the decide the mode to all the blocks based thereon. The picture elements of the input picture signal are thinned out for every block according to the decided mode". Here, an interpolation signal for respective modes of interpolations are calculated to be compare to the original pixel value to decide which mode of interpolation to use for picture elements in every block**) and sending each interpolation candidate data from the interpolation circuit for each unknown interpolation data to an output circuit (**Page 10, "the pixel information and mode information are output to the reception side."**);

a determining circuit (**Drawing 2, Unit 20**) for selecting one of the interpolation methods based on a difference between the test interpolation data and actual pixel data of said plurality of normal pixels and providing a selection signal to said output circuit (**Abstract, "Then, the sum in the block of the absolute value of the difference between an interpolation signal and an original signal, namely, the quantity of the distortion to the respective modes for every block is calculates the decide the mode to all the blocks based thereon"**); and

an output circuit for outputting the interpolation candidate data calculated by the selected interpolation circuit as the interpolation pixel data according to the selected signal (**An interpolation unit on a reception side, see Page 10, "Lastly, the pixels in the input**

image signal are thinned for each block according to the mode selected in (11) (12), the pixels are rearranged, and the pixel information and mode information are output to the reception side. On the reception side, pixel interpretation based on the mode information which has been sent is performed to reconstruct the image").

The evidence of inherency that ***Ashibe***, which performs block based processing, interpolates the same unknown interpolation pixel for each unknown interpolation pixel base on calculations performed on test interpolation data of a plurality of normal pixel neighboring the interpolation pixel, is provided by ***Saver*** (**Abstract and Fig 2**).

For arguments sake, even if ***Ashibe*** does not inherently perform the process for the reasons and evidences set forth by the examiner, one of ordinary skill at the time of the invention would've look to ***Saver*** to adopt its method of pixel compression / thinning and pixel interpolation on a pixel by pixel basis within a block of M x M pixels because it provides valid thinning and interpolation processes that is required by ***Ashibe***.

While the interpolation unit of ***Ashibe*** independently calculates interpolation candidate data of the same interpolation pixel using respective different interpolation methods, ***Ashibe*** does not disclose the internal structure of said unit comprise a plurality of independent interpolation circuits.

Jiang discloses an interpolation circuitry configuration that takes edge direction into consideration when performing interpolation (**See Figs 1-2**) having an internal structure comprising a plurality of interpolation circuits with specific logic components each independently calculates interpolation candidate data (**Fig 8, Adder Logic 88 and Division**

Logic 90) of a same pixel to be interpolated (**Fig 1, Pixel to be interpolated**), using different interpolation methods (**Col 13, Rows 48-58**).

Jiang demonstrated that it is well known in the art to implement separate sets of logic to form independent circuits to each perform its respective interpolation methods, it would've been obvious to one of ordinary skill in the art at the time of the invention to design the internal circuitry of interpolation unit of ***Ashibe*** with independent circuits to calculate respective correlation values of respective different interpolation methods such that its intended function as disclosed would be successfully implemented.

Regarding Claims 2 and 5, ***Ashibe*** discloses wherein the determining circuit calculates a evaluation data for each of the interpolation circuits, by summing up the absolute values of the difference between the test interpolation data and the actual pixel data, and selects one of the interpolation circuits based on the evaluation data (**Abstract, "Then, the sum in the block of the absolute value of the difference between an interpolation signal and an original signal, namely, the quantity of the distortion to the respective modes for every block is calculates the decide the mode to all the blocks based thereon"**).

Regarding Claims 3 and 6, ***Ashibe*** discloses wherein the determining circuit calculates binarized or ternarized values of the difference between the test interpolation data and the actual pixel data (**Drawing 3 (c), at least two or more sets of neighboring "o" are used to calculate a specific "x"**).

Regarding Claim 7, ***Ashibe*** does not disclose that the pixel interpolation circuit is within an image scanner.

Saver discloses such configuration (**Fig 1A, Corneal Image System with a CCD camera module 110**).

Therefore, one possible implementation of the combination would be a scanner system the likes of ***Saver*** where image data is compressed and store into a memory. When the user require the image be outputted by an output unit (**for example, display or printer**), it is interpolated by a scanner processor (**Col 9, Rows 10-12**). In this way, memory storage is conserved and an apparatus or circuit as required by the claims is obtained.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Richard Z. Zhu whose telephone number is 571-270-1587 or examiner's supervisor King Y. Poon whose telephone number is 571-272-7440. Examiner Richard Zhu can normally be reached on Monday through Thursday, 0630 - 1700.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Richard Z. Zhu/
Assistant Examiner
Art Unit 2625
05/14/2010

/King Y. Poon/
Supervisory Patent Examiner, Art Unit 2625